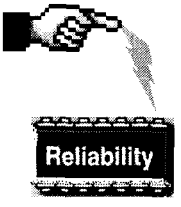
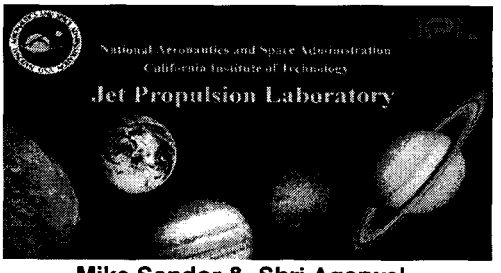
Military & Aerospace/Avionics COTS Conference

August 22-25, 2000

Commercial Off-The-Shelf (COTS) Program

ESD LATENCY - Reliability Investigation & Analysis





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AGENDA

- Background Investigation
- Experimental Approach
- ESDL Data & Failure Analysis
- Conclusions
- Recommendations

ACKNOWLEDGEMENT

The work was performed at
Jet Propulsion Laboratory
California Institute of Technology
under contract to the
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ESDL CONCERN FOR SPACE HARDWARE

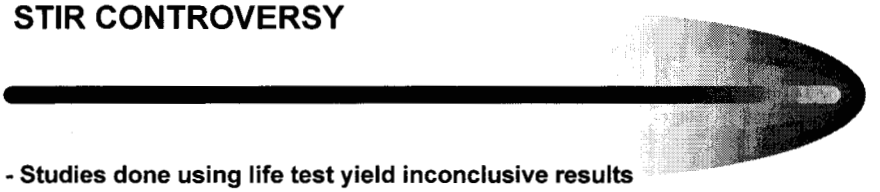
Flight board or circuit card assemblies suspected and or confirmed of being exposed to ESD may not be reliable because of latent damage.

Because of different ESD tolerance of components there is no way of identifying which components have been affected except by testing at the component level.

The issue at hand:

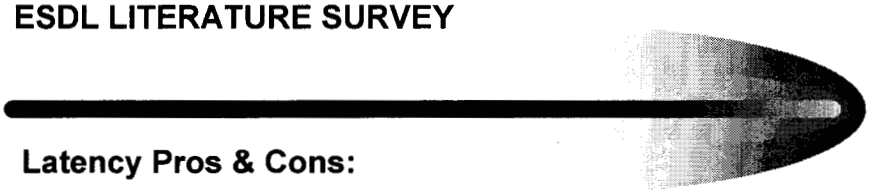
Is the ESDL reliability concern being overstated if board level testing passes ?

ESDL STUDIES STIR CONTROVERSY



- **Studies done using life test yield inconclusive results**
- **Most latent failures are simply leak pins**
- **On-chip protection negates further degradation**
- **Possibility of receiving a stress large enough to cause damage but small enough not to destroy is remote**
- **Unlikely that degradation will worsen over the operational life of the device**
- **ESDL physics is not well understood**
- **Experiments have proved inconclusive**
- **Little rigorous work done on latency**

ESDL LITERATURE SURVEY



Latency Pros & Cons:

General EOS/EQD Equation - **No**

VLSI Circuits Degrade Due To ESD Stress Below ESD Rating Voltage -**Yes**

CDM Only Reproducible Field Degradation and Its Reliability Aspect - **Yes**

Characterization and Failure Analysis of Advanced CMOS Sub-Micron Structures -**No**

ESD Latency Effects in CMOS Integrated Circuits - **Yes**

Metallurgical Study of ESD Damage in DRAM - **Yes**

ESD Sensitivity and Latency Effects of Some HCMOS ICs - **Yes**

Investigation of Latent Failures Due to ESD in CMOS ICs - **Yes**

Event-Dependent ESD Latent-Failure Behavior of Bipolar ICs - **Inconclusive**

Latency and the Physical Mechanisms Underlying Gate Oxide Damage - **Yes**

ESD DEFINITION

Electrostatics:

Static charge buildup (- or +) from the "triboelectric" effect that occurs when two dissimilar materials are rubbed together.

A person walking across a carpet can produce electrostatic charges on the human body up to 35,000 volts.

Electrostatic Discharge (ESD):

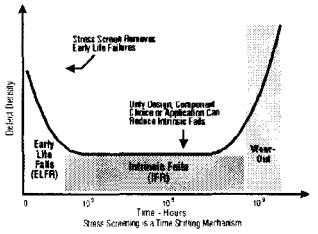
Electrostatic charge buildup that is dissipated to another object that has less charge - a grounded object e.g. grounded doorknob

ESDLatency DEFINITION(s)

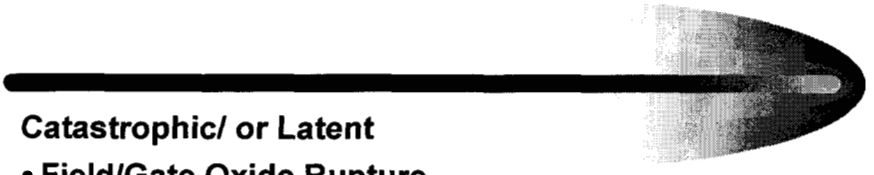
1. ESDL failure is defined as a flaw in the structure that is not apparent at the time of its onset, but that will reveal itself by facilitating a hard failure at a subsequent, normally nonfatal stress to which the device is subjected during ordinary use.

2. An ESD induced defect which does not initially cause an out-of-spec condition but does cause a reliability failure during operational life.

3. ESDL ⟷ A Walking Wounded Device that can fail anytime during early life or operating life.



POTENTIAL FAILURE MECHANISMS/MODES FROM ESD



Catastrophic/ or Latent

- Field/Gate Oxide Rupture
- Dendrite Formation
- Hot Spots due to silicon damage
- Melted Channels (connecting hot spots)
- Increased Leakage Current
- Junction Burnout/Drain-Source Short
- Risetime Effects (timing)
- Hot Carrier Reduced Lifetime
- TDDB Reduced Lifetime
- Enhanced Interconnect Electromigration (see attach A)
- Resistor Damage

EXPERIMENTAL APPROACH TAKEN

EXPERIMENTAL PART CANDIDATES

Three Scaled Devices Chosen:

Devices:	Memory	Buffer	Buffer
Size:	4u	3u	1.25u
Package:	DIP	DIP	DIP
SS:	100	100	100

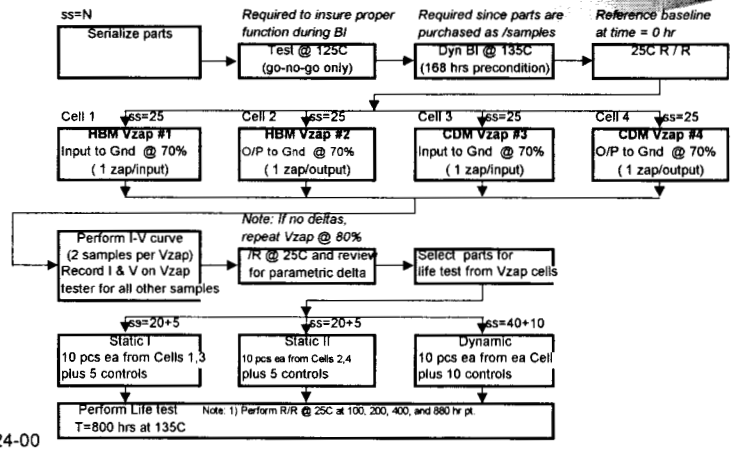
"Standard scaling practices, while optimized for device operation to process logic, have often been shown to have a negative impact on ESD performance".

Ref: SEMATECH TT 98013452A-TR

However, we believe that the process & design protection circuits play a vital role as well.

EXPERIMENTAL DESIGN

FLOW:

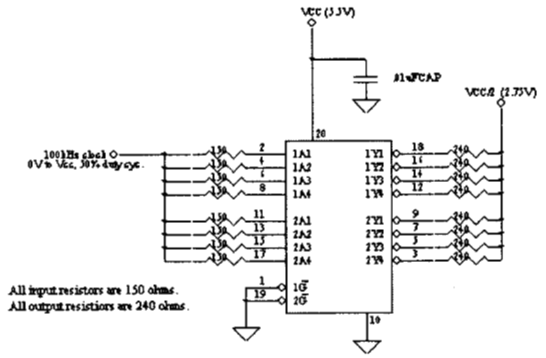


ESDL ACCELERATED STRESS CONDITIONS

Life Test Circuit

Outputs are under load

Inputs are not under load



Dynamic Burn-in condition.

ESD SIMULATION METHODs

There are a number of ESD sources:

Charged Human Body Model (HBM) Chosen*

- Reliable and repeatable test results, quantitative measurements
- Automatic testing with read/record, programmable tester

Charged Objects (Machine Model)

Charged Devices (Charged Device Model)

Charged Boards

Charge Surface (EMI Charged Spacecraft)

Electromagnetic Pulse

*Reference test method EIA/JESD22-A114-A

A Static Charged Human Can Reach 35,000 Volts!

Susceptibility Ranges of Devices Exposed to ESD From a Person:

MOSFET	100 - 200V
GaAsFET	100 - 300V
JFET	140 - 10,000V
CMOS	250 - 3000V
Schottky Diodes	300 - 2,500V
Bi-Polar Transistors	380 - 7,000V
Op Amp	190 - 2500V
ECL	500 - 1500V
SCR	680 - 1,000V

Classification Criteria:

Class 1 - ≤ 2000 Fails

Class 2 - ≥ 2000 ≤ 4000 Passes

Class 3 - ≥ 4000 Passes

EXPERIMENTAL DATA

Test Intervals:
Pre-ESD, Post Burn-in @ 200, 400, 800 and 1700 hours

Monitored Test Parameters:**

- Input current low and high
- Output current low and high
- Shorted output current
- Propagation delays
- Quiescent supply current
- Operating current
- Leakage current
- Three-state output leakage current, output high and low
- Protection diode voltage
- Functionality

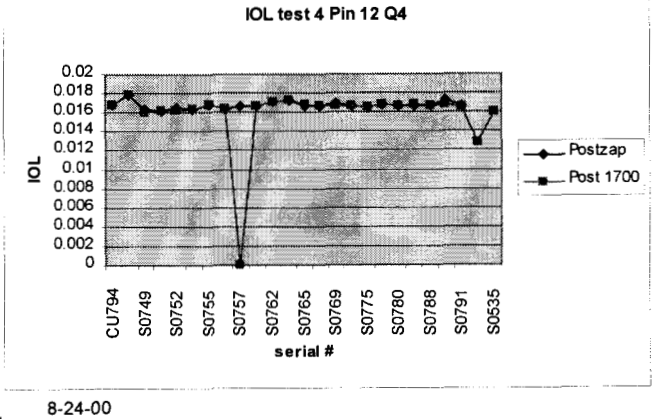
**>32,000 measurements per part type

FAILURE ANALYSIS

ESDL ELECTRICAL SIGNATURE

Example 1

Output Fails Catastrophic @ <200 hrs Operation



SO757-IOL P12 Q4

PreBi = 16.2 ma

168 BI = 16.6 ma

Post Zap = 16.6 ma

200 hrs = 0.2 ma

400 hrs = 0 ma

800 hrs = 0 ma

1700 hrs = 0 ma

ESDL ELECTRICAL SIGNATURE

Example 2 & 3

Output Fails Catastrophic @ <200 hrs Operation

ESD damage prior to BI is evident.

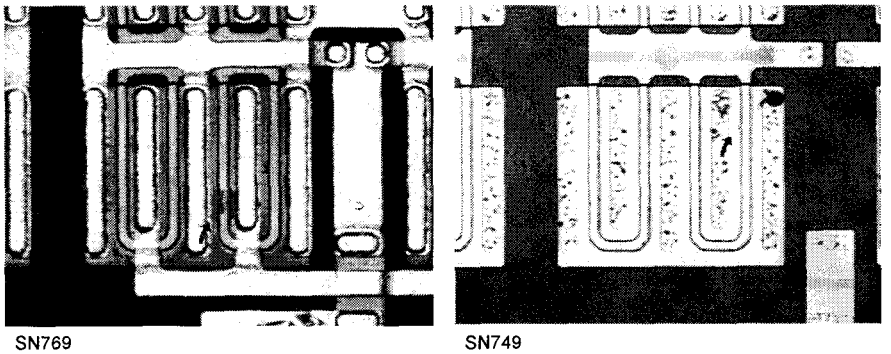
SO757-IOL P18 Q1	SO769-TPZL P9 Q5
PreBi = 54.6 ma	PreBi = 12.6 ns (max limit=21 ns)
168 BI = 56.0 ma	168 BI = 12.5 ns
Post Zap = 16.0 ma	Post Zap = 12.5 ns
200 hrs = 0 ma	200 hrs = 100 ns (beyond scale)
400 hrs = 0 ma	400 hrs = 100 ns
800 hrs = 0 ma	800 hrs = 100 ns
1700 hrs = 0 ma	1700 hrs = 100 ns

Evidence of Latent Damage

TYPICAL OUTPUT ESD DAMAGE (HBM)

Source to Drain short at output enable buffer

Source to Drain short at output enable buffer

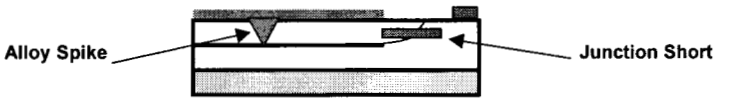


SN769 SN749

Note: Liquid crystal analysis showed that Icc current was flowing in the n-channel

OUTPUT ESD LATENCY DAMAGE MECHANISM

Junction Burnout (short) Model



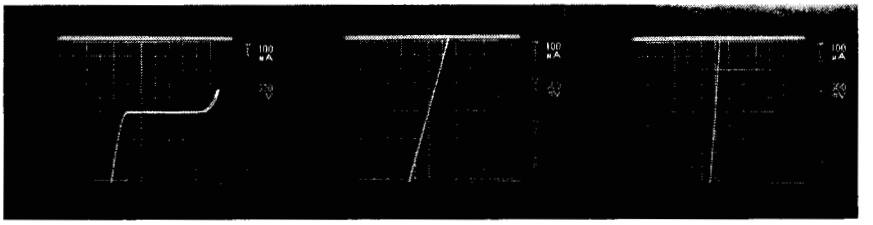
Junction burnout is caused by injection of an ESD transient of sufficient energy and duration to initiate second breakdown. Subsequent to second breakdown the junction melts or a metal spike can grow from the metallization through the junction. Junction burnout usually results in a high reverse leakage current or a total short.

*Pj = IV_{BD} * Tj = Tc *Resulting in Junction Short

Note with ESD latency it is postulated that the second breakdown is not immediate nor permanent but damage has occurred. Under continue operation and current more energy is dissipated, increasing the temperature until the overstress ends.

TYPICAL INPUT ESD DAMAGE (HBM)

Electrical Signature of Failed Inputs

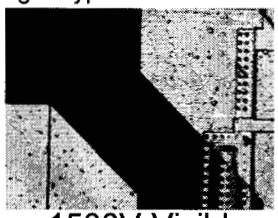


Curve tracer curves. Photo left is typical of a good input. Photo center is the shorted (2K ohm) S/N S0565 pin-15, and photo right is the shorted (368 ohm) S/N S0568 pin-4.

TYPICAL INPUT ESD PHYSICAL DAMAGE (HBM)

Input Polysilicon Resistor Damage: Typical failure is short to Vcc & open

1000V-Not Visible

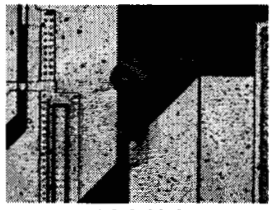


1500V-Visible

2000V

3000V

3500V



4000V

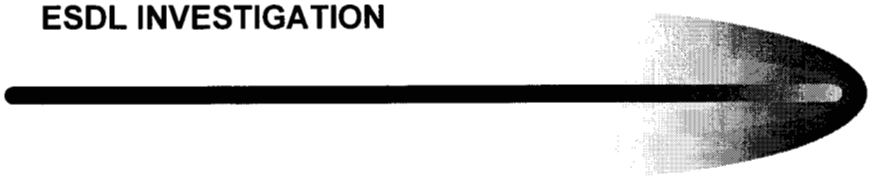
POLYSILICON RESISTOR DAMAGE ANALYSIS

ESD input protection resistors used are typically series elements - diffused or polysilicon

- Diffused resistors can be advantageous because the parasitic diode inherent in the structure dissipates some energy into the substrate
- Polysilicon resistors are electrically isolated from the substrate therefore all of the energy is dissipated in the resistor which can lead to damage in the resistor itself

Ref: "A design Methodology for ESD Protection Networks," Proc. 1985 EOS/ESD Symp.

CONCLUSIONS FROM ESDL INVESTIGATION



ESD Latent damage may be detectable by its electrical signature but its lifetime behavior is not predictable. Latent damage can result in permanent failure under some stress conditions and thereby poses a reliability concern. Device outputs with latent damage can fail if subjected to stress such as current loading. However, inputs with latent damage seem less likely to fail if they are under nominal electric fields. This is highly dependent on where the damage resides. Input resistors are likely to be more immune to latent failure than damaged junctions or gate oxides. This experiment did not validate any lifetime latent failures on the inputs exposed to low ESD.

RISK MITIGATION USED on PARTS EXPOSED to ESD

Recommendations:

1. Test parts 100% (DC/AC) @ 25 C with R/R
2. Use IDDQ test where possible
3. Reject parts that are outliers or do not fall within 1 sigma of parametric distribution
4. Screen parts 100% with 240 hr dynamic BI
5. Repeat steps 1 and 3

Perform FA on known ESD parts to gain added information e.g. I/Os & Inputs failure mechanism

RISK MITIGATION USED on CCA Exposed to ESD

Recommendations:

Option A

1. **Remove & test I/O parts 100% (DC/AC) @ 25 C with R/R**
2. **Use IDDQ test where possible**
3. **Reject parts that are outliers or do not fall within 1 sigma of parametric distribution**

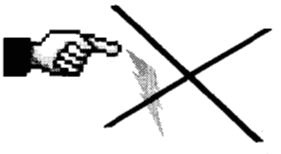
Option B

4. **Screen CCA(s) 100% with min 240 hr dynamic BI**
5. **Reject CCA(s) that do not fall within 1 sigma of expected performance goals**

Option C

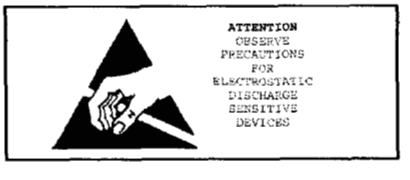
1. **Replace CCA with new one**

PREVENTING ESD/ESDL is SERIOUS BUSINESS!



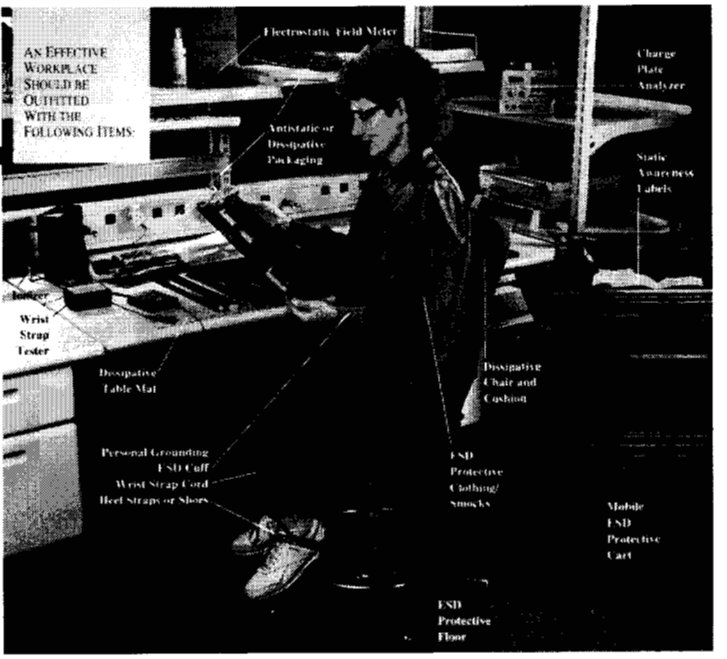
Environment/Handling Requirements:

- Wrist Straps
- Anti-static smocks
- Anti-static gloves & finger cots
- Dissipative table tops and mats
- Grounded tip soldering irons
- Grounded stools and chairs
- Anti-static & shielded bags
- Protective tote boxes
- Protective DIP tube & magazines
- Grounded carts
- Humidity control
- Air Ionization
- Voltage suppressors
- Conductive floor tiles
- Shoe grounding straps
- Edge connector shorting bars



Reference ESD Control Standard: ANSI/ESD S20.20-1999

ESD Protected Workstation



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Source: Intel Corporation

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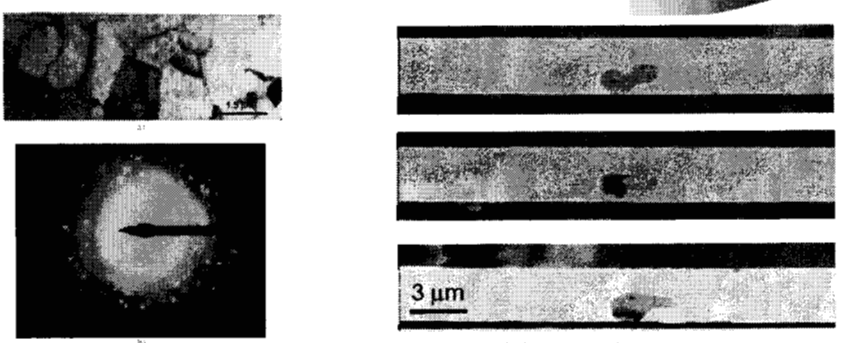
Attachment A

Example of Pulsed ESD Latent Damage in AlCu line



The mean EM lifetime was reduced by a factor of 4

Ref Microanalysis of VLSI Interconnect Failure Modes under Short-Pulse Stress Conditions; IRPS 2000

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RECOMMENDATIONS for FUTURE WORK

1. Additional characterization for different technologies and design schemes to better understand and possibly predict the reliability of latent damage
2. Establish an ongoing database with industry and others to identify component ESD tolerance levels